IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 1, between lines 19-21 of the specification with the following:

An object of the invention is to enhance a flexibility of parallel data processing. ~~To this end, the invention provides a device, a camera system and a method as defined in the independent claims. Advantageous embodiments are defined in the dependent claims.~~

Replace the paragraph spanning pages 5-6, between page 5, line 22, and page 6, line 8 of the specification with the following:

Fig. 3 shows a practical implementation of a processor array LPA 1...320. By left and right communication channels COMM and multiplexers MUX1...320, each processing element can directly obtain data from six columns. The data read from the line memory LM or a given TSMM can be redirected to the corresponding processing element or to the processing element at the left or the right thus

providing limited communication between processing elements LPA1...320. One word of data can be shifted to the neighboring processing elements in a given clock cycle. All processing elements are running identical instructions on their local data. Again, power consumption is reduced compared to a sequential column processor, because the control and address-decoding is performed only once and shared by all processing elements according to a Single Instruction Multiple Data (SIMD) principle. Each processor comprises an accumulator ACC1...320 that stores the latest result, which can be used as an operand for a next instruction. Both an adder and a multiplier are implemented in the ALU1...320 and with these functions comparison, addition, subtraction, data weighing and multiply-accumulate are performed. The processors incorporate a flag F that is set according to the latest result. Based on this flag F conditional pass-instructions are possible, allowing a limited form of data-dependency in the algorithms. All 320 flags F1...F320 are connected to a global line EVT, which is coupled to the CPU. In this way, iteration processes with a certain end-condition can be run on the parallel processor array LPA, or the CPU can react on image contents. The CPU therefore provides a

control signal INSTR. Resulting data becomes available at points P1...~~P4~~P320. Data from the line memory LM or from the TSMM coupled to these points P1...P4 may be used in the respective processing elements LPA1...320.

Replace the paragraph on page 8, between lines 10-19 of the specification with the following:

Fig. ~~9 shows~~ 8 shows a processor selective access mode. This figure shows the ability of using the TSMM to randomly access one of the four outputs of the processor and store the output randomly in one of the four registers of a column of the TSMM. As an example, the switch T at P2 is closed, therefore only allowing the data from LPA2 to enter the TSMM. By activating appropriate switches T, this data is routed to the fourth register MR in the first column of the TSMM. In this way, an output from the LPA2 is written in the fourth register of the first column c1 of the TSMM. Reading by a processing element from the TSMM will cause problems because the LPA1...320 are not individually selectable. All processing elements will then try to read and perform some processing with uncertain results. When the accumulators of the

LPA1...320 are selectively addressable, this problem is effectively solved.